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10/715,064	11/17/2003	**Anand Pande**	15156US01	7036

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EXAMINER	
TSAI, SHENG JEN	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/715,064	PANDE, ANAND	
	Examiner	Art Unit	
	SHENG-JEN TSAI	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/17/2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is taken in response to Applicant's Request for Continued Examination (RCE) filed on September 17, 2008 regarding application 10/715,064 filed on November 17, 2003.

2. Claims 1-11 have been cancelled.

Claims 12-17 have been added.

Claims 12-17 are pending for consideration.

3. ***Response to Remarks***

Applicants' amendments and remarks have been fully and carefully considered.

(1) In response, a new ground of claim analysis based on a newly identified reference (Burns et al., US 4,528,665) has been made.

(2) In addition, another claim analysis based on a previously relied-on reference (Cohn) has also been made.

Applicants contend that the Cohn reference fails to teach the limitation "(d) repeating ..." because "adding the gray code word to every linear code word does not produce addresses that satisfy the one bit difference property."

It should be noted that the claims merely recite "selecting D addresses from N generated addresses" and that "the selected D addresses satisfy the one bit difference property."

Cohn teaches generating N addresses [N-K Gray coded addresses plus K zero fillers as shown in figure 1, which makes a total of N generated addresses], and the corresponding selected D addresses are the N-K Gray coded addresses [figure 1, 2;

thus D = N-K]. The Gray coded addresses satisfy the one bit difference property [figure 2 shows a case of gray code with D=32, note that they satisfies the one bit difference property; A Gray code is a sequence of binary words of the same dimension in which adjacent words, and the first and last words are Hamming distance 1 apart. For example, the following is a Gray code of dimension 3 ... Any two adjacent words, and the first and last words, differ in only one position, thereby being Hamming distance 1 apart. Such codes may be constructed for any dimension (col. 2, lines 51-67)].

Also noted that the generating and selecting of the Gray code sequence is done totally independent of the linear coder.

Thus, Cohn's disclosure clearly meets all the limitations recited in claim 12 as currently amended.

(3) Refer to the corresponding sections of the following claim analysis for details.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 12-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Each of independent claims 12 and 15 recites "(a) generating a sequence of binary addresses with a length N." However, this limitation may either be interpreted as "a sequence of N binary addresses," or be interpreted as "each of the binary addresses is of N-bit long." Clarification is needed.

For the purpose of claim analysis with respect to prior art, the Examiner interprets this limitation as "a sequence of N binary addresses."

Each of independent claims 12 and 15 also recites "(b) selecting a combination of D addresses from the generated sequence." The word "combination" may be reasonably interpreted as "D addresses from the generated sequence are combined in certain ways to form a combined address," but the Specification suggests actually no "combination" is performed. Clarification is needed.

For the purpose of claim analysis with respect to prior art, the Examiner interprets this limitation as "selecting a group of D addresses from the generated sequence," or "selecting a set of D addresses from the generated sequence."

Claims 13-14 are rejected by virtue of their dependency from claim 12.

Claims 16-17 are rejected by virtue of their dependency from claim 15.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 12, 14-15 and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Burns et al. (US 4,528,665, hereinafter referred to as Burns).

As to claim 12, Burns discloses **a circuit** [as shown in figures 1A and 1B] **comprising**:

a processor [… to generate sequential addresses comprised of binary digits (bits) for accessing a memory for reading out stored instruction words sequentially for a binary digital data processing system (col. 1, lines 19-23)]; **and**

a memory connected to the processor [… to generate sequential addresses comprised of binary digits (bits) for accessing a memory for reading out stored instruction words sequentially for a binary digital data processing system (col. 1, lines 19-23); memory units, figure 1A, 10], **said memory storing a plurality of instructions** [… to generate sequential addresses comprised of binary digits (bits) for accessing a memory for reading out stored instruction words sequentially for a binary digital data processing system (col. 1, lines 19-23)], **wherein execution of the instructions by the processor causes**:

(a) **generating a sequence of binary addresses with a length N** [figure 2 shows 32 (N=32) gray-code addresses denoted as B4B3B2B1B0; Gray code counter means for generating said memory addresses to be refreshed in a predetermined sequence wherein no more than one binary digit is altered to form successive ones of said memory addresses to be refreshed (claim 2)], **wherein N is greater or equal to a desired sequence length D** [the corresponding D addresses are the 32 (D=32) gray-code addresses denoted as B4B3B2B1B0], **wherein N is a power of 2** [32 is a power of 2];

(b) **selecting a combination of D addresses from the generated sequence** [the corresponding D addresses are the 32 (D=32) gray-code addresses denoted as B4B3B2B1B0];

(c) **checking if the addresses in the selected combination satisfy the property of only one bit difference between consecutive addresses** [as shown in figure 2, where the 32 gray-code addresses satisfy the property of only one bit difference between consecutive addresses]; **and**

(d) **repeating (b) and (c) until a combination of D addresses that satisfies the one bit difference property is found** [the corresponding D addresses are the 32 (D=32) gray-code addresses denoted as B4B3B2B1B0 as shown in figure 2, where the 32 gray-code addresses satisfy the property of only one bit difference between consecutive addresses].

As to claim 14, Burns teaches that **D is the depth of a data structure** [the corresponding data structure is the memory units (figure 1A, 10); Gray code counter means for generating said memory addresses to be refreshed in a predetermined sequence wherein no more than one binary digit is altered to form successive ones of said memory addresses to be refreshed (claim 2)].

As to claim 15, it recites substantially the same limitations as in claim 12, and is rejected for the same reasons set forth in the analysis of claim 12. Refer to "As to claim 12" presented earlier in this Office Action for details.

As to claim 17, it recites substantially the same limitations as in claim 14, and is rejected for the same reasons set forth in the analysis of claim 14. Refer to "As to claim 14" presented earlier in this Office Action for details.

8. Claims 12-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohn et al. (US 4,556,960, hereinafter referred to as Cohn).

As to claim 12, Cohn discloses **a circuit** [figure 1 shows the circuit] **comprising**:

a processor [the present invention relates generally to the sequential allocation of addresses in a computer memory, and more specifically, to such an allocation which mitigates the damage resulting from hardware or software errors by reducing the possibility of relatively recent data being overwritten (column 1, lines 7-13); figure 1; it is inherent that a processor (or CPU) is included in a computer to perform the generation of addresses and other tasks]; **and**

a memory connected to the processor [the memory unit (figure 1, 7); the present invention relates generally to the sequential allocation of addresses in a computer memory, and more specifically, to such an allocation which mitigates the damage resulting from hardware or software errors by reducing the possibility of relatively recent data being overwritten (column 1, lines 7-13)], **said memory storing a plurality of instructions** [the present invention relates generally to the sequential allocation of addresses in a computer memory, and more specifically, to such an allocation which mitigates the damage resulting from hardware or software errors by reducing the possibility of relatively recent data being overwritten (column 1, lines 7-13)], **wherein execution of the instructions by the processor causes**:

(a) generating a sequence of binary addresses with a length N [the corresponding sequence of binary address comprises the Gray Coder sequence (figure 1, 2) which has a length of N-K, and the zero filler sequence (figure 1, 5) which has a length of K; thus a total length of N as shown in figure 1], **wherein N is greater or equal to a desired sequence length D** [the corresponding desired sequence of length D is the

Gray Coder sequence (figure 1, 2) which has a length of N-K as shown in figure 1, in other words, D = N-K; note that N is greater than or equal to N-K], **wherein N is a power of 2** [the 2^n addresses ... (col. 4, lines 59-67)];

(b) selecting a combination of D addresses from the generated sequence [the corresponding group of D addresses are the Gray Coder addresses (figure 1, 2) which has a length of N-K as shown in figure 1, in other words, D = N-K];

(c) checking if the addresses in the selected combination satisfy the property of only one bit difference between consecutive addresses [figure 2 shows a case of gray code with D=32, note that they satisfies the one bit difference property; A Gray code is a sequence of binary words of the same dimension in which adjacent words, and the first and last words are Hamming distance 1 apart. For example, the following is a Gray code of dimension 3 ... Any two adjacent words, and the first and last words, differ in only one position, thereby being Hamming distance 1 apart. Such codes may be constructed for any dimension (col. 2, lines 51-67)]; and

(d) repeating (b) and (c) until a combination of D addresses that satisfies the one bit difference property is found [figure 2 shows a case of gray code with D=32, note that they satisfies the one bit difference property; A Gray code is a sequence of binary words of the same dimension in which adjacent words, and the first and last words are Hamming distance 1 apart. For example, the following is a Gray code of dimension 3 ... Any two adjacent words, and the first and last words, differ in only one position, thereby being Hamming distance 1 apart. Such codes may be constructed for any dimension (col. 2, lines 51-67)].

As to claim 13, Cohn teaches that **D is an odd number** [A Gray code is a sequence of binary words of the same dimension in which adjacent words, and the first and last words are Hamming distance 1 apart. For example, the following is a Gray code of dimension 3 ... Any two adjacent words, and the first and last words, differ in only one position, thereby being Hamming distance 1 apart. Such codes may be constructed for any dimension (col. 2, lines 51-67)].

As to claim 14, Cohn teaches that **D is the depth of a data structure** [figure 1, 5 shows the data structure of N-K positions for generating Gray Code, figure 1 also shows that N-K is the length of the data structure of the address index input with N-K positions; figure 2 shows an example of the generated Gray Code].

As to claim 15, it recites substantially the same limitations as in claim 12, and is rejected for the same reasons set forth in the analysis of claim 12. Refer to "As to claim 12" presented earlier in this Office Action for details.

As to claim 16, it recites substantially the same limitations as in claim 13, and is rejected for the same reasons set forth in the analysis of claim 13. Refer to "As to claim 13" presented earlier in this Office Action for details.

As to claim 17, it recites substantially the same limitations as in claim 14, and is rejected for the same reasons set forth in the analysis of claim 14. Refer to "As to claim 14" presented earlier in this Office Action for details.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 13 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Burns et al. (US 4,528,665, hereinafter referred to as Burns), and in view of Cohn et al. (US 4,556,960, hereinafter referred to as Cohn).

As to claim 13, Burns does not teach that the length D is an odd number.

However, Cohn explicitly teach that D is an odd number [A Gray code is a sequence of binary words of the same dimension in which adjacent words, and the first and last words are Hamming distance 1 apart. For example, the following is a Gray code of dimension 3 ... Any two adjacent words, and the first and last words, differ in only one position, thereby being Hamming distance 1 apart. Such codes may be constructed for any dimension (col. 2, lines 51-67)].

Therefore, it would have been obvious for one of ordinary skills in the art at the time of Applicants' invention to have recognize that the length D of a Gray code sequence may be an odd or an even number, as demonstrated by Cohn, hence lacking patentable significance.

As to claim 16, it recites substantially the same limitations as in claim 13, and is rejected for the same reasons set forth in the analysis of claim 13. Refer to "As to claim 13" presented earlier in this Office Action for details.

11. ***Related Prior Art of Record***

The following list of prior art is considered to be pertinent to applicant's invention, but not relied upon for claim analysis conducted above.

- Hsu et al., (US 6,845,414), "Apparatus and Method of Asynchronous FIFO Control."
- Camilleri et al., (US 6,434,642), "FIFO Memory System and Method with Improved Determination of Full and Empty Conditions and Amount of Data Stored."
- Shyi et al., (US 5,426,756), "Memory Controller and Method Determining Empty/Full Status of a FIFO Memory Using Gray Code Counters."
- Brooks et al., (US 5,410,664), "RAM Addressing Apparatus with Lower Power Consumption and Less Noise Generation."
- Jiang, (US Patent Application Publication 2004/0207547), "Method of Scalable Gray Coding."
- Pontius, (US 6,337,893), "Non-Power-Of-Two Gray-Code Counter System Having Binary Incrementer with Counts Distributed with Bilateral Symmetry."
- Yi, (US 6,703,950), "Gray Code Sequences."

Conclusion

12. Claims 12-17 are rejected as explained above.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sheng-Jen Tsai whose telephone number is 571-272-4244. The examiner can normally be reached on 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim can be reached on 571-272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Sheng-Jen Tsai/

TFSA Examiner, Art Unit 2186

November 14, 2008